

Correction Magnet Power Supplies for APS Machine

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1. INTRODUCTION

A number of correction magnets are required for the advanced photon source (APS) machine to correct the beam. There are five kinds of correction magnets for the storage ring, two for the injector synchrotron, and two for the positron accumulator ring (PAR). Table I shows a summary of the correction magnet power supplies for the APS machine. For the storage ring, the displacement of the quadrupole magnets due to the low frequency vibration below 25 Hz has the most significant effect on the stability of the positron closed orbit. The primary external source of the low frequency vibration is the ground motion of approximately 20 μm amplitude, with frequency components concentrated below 10 Hz. These low frequency vibrations can be corrected by using the correction magnets, whose field strengths are controlled individually through the feedback loop comprising the beam position monitoring system.

A total of eighty correction magnets are distributed around the injector synchrotron ring. These magnets provide the field changes required for the beam orbit correction during the acceleration period at the rate of 2 Hz. Since the exact field correction required at each correction magnet location will not be known until a beam is actually accelerated, an arbitrary function generator (AFG) [1] is required to produce a correction field.

The correction field required could be either positive or negative. Thus for all the correction magnets, bipolar power supplies (BPSs) are required to produce both polarities of correction fields. Three different types of BPS are used for all the correction magnets. Type I BPSs cover all the correction magnets for the storage ring, except for the trim dipoles. The maximum output current of the Type I BPS is 140 Adc. A Type II BPS powers a trim dipole, and its maximum output current is 60 Adc. The injector synchrotron and PAR correction magnets are powered from Type III BPSs, whose maximum output current is 25 Adc.

2. CIRCUIT CONFIGURATION

Figure 1 shows the simplified circuit configuration of a bipolar power supply. The topology is a full-bridge dc-to-dc converter. The switching frequency is 20 kHz synchronized with the main clock. The regulation is achieved by controlling the pulse width. Power MOSFETs are considered for the switching devices due to their excellent switching characteristics and easier drive. Another advantage of using power MOSFET is that the new generation of power MOSFETs allows us to utilize their inherent body diodes for the anti-parallel diodes of the switches. L_m and R_m represent the inductance and resistance of a correction magnet. For positive magnet current, switches S1 and S4 are closed. Only the upper switch S1 is controlled according to the pulse width modulation (PWM) signal, while the bottom switch S4 remains closed. When S1 is opened, the magnet current decays through the still closed switch S4 and diode D3. However, double gating, which controls both S1 and S4 simultaneously, may be required to keep di/dt constant around zero. For negative current, switches S2 and S3 and diode D4 are used in a similar fashion. In order to regulate the magnet current, the magnet current information is fed back to an error amplifier input via a current measuring device as the feed back signal, V_f , and is compared with the reference voltage, V_r , provided by a digital-to-analog converter (DAC). The current measuring device considered is either a shunt resistor or a zero-flux current transductor (CT). Since the current loop has slow response to the input voltage variation due to the large time constant of a correction magnet, the voltage-feedforward technique, which varies the ramp slope, will be used in the regulator circuit for constant volt-second operation to the input variation. The unregulated dc input bus voltage, V_{in} , is provided by a separate ac/dc rectifier.

3. ANALYSIS OF THE MAIN POWER CIRCUIT

Referring to Figure 1, the steady-state analysis of the circuit for positive magnet current is carried out as follows:

A. For $0 \leq t \leq T_{on}$: (T_{on} = the conduction time of both switches S1 and S4)

Figure 2 (a) shows the equivalent circuit when switches S1 and S4 are turned ON. Then, we can write a differential equation as

$$V_{in} = L_m \frac{di(t)}{dt} + R_m i(t) + 2V_Q \quad (1)$$

where V_Q = forward voltage drop of a switch.

By solving (1) for the current $i(t)$, we get

$$i(t) = \frac{V_{in} - 2V_Q}{R_m} (1 - e^{-\tau t}) - I_{L0} e^{-\tau t} \quad (2)$$

where I_{L0} = initial magnet current at $t = 0$ and $\tau = \frac{R_m}{L_m}$.

B. For $T_{on} \leq t \leq T_s$: (T_s = one switching period, 50 μs)

During this period Switch S4 remains ON and the anti-parallel diode D3 is conducting. Then the magnet current freewheels, and the equivalent circuit is shown in Fig. 2 (b). Thus, an equation for this period can be written as

$$0 = L_m \frac{di(t)}{dt} + R_m i(t) + V_Q + V_D \quad (3)$$

where

V_D = forward voltage drop of a diode.

The solution of (3) for $i(t)$ is given by

$$i(t) = I_{L1} e^{-\tau t} - \frac{V_Q + V_D}{R_m} (1 - e^{-\tau t}) \quad (4)$$

where I_{L1} = magnet current at $t = T_{on}$.

The average voltage of the magnet, $V_{o(dc)}$, is determined by

$$\begin{aligned} V_{o(dc)} &= (V_{in} - 2V_Q) \delta - (V_Q + V_D)(1 - \delta) \\ &= (V_{in} + V_D - V_Q) \delta - (V_Q + V_D) \end{aligned} \quad (5)$$

where $\delta = \text{duty ratio} = \frac{T_{\text{on}}}{T_s}$

Note that the minimum input bus voltage is roughly determined from (5), by assuming that $V_Q = V_D$ and duty ratio δ is 50 % at minimum input voltage.

$$V_{\text{in (min)}} = 2V_{\text{o(dc),max}} - 4V_Q \quad (6)$$

$$= 2I_{\text{o(max)}} R_m - 4V_Q \quad (7)$$

where $I_{\text{o(max)}} = \text{maximum dc magnet current.}$

4. CONTROL

4.1 Control for storage ring correction magnets

Figure 3 shows the simplified block diagram of a control scheme of correction magnet power supplies for the storage ring . PSCU is the power supply control unit which contains the intelligence that interfaces directly to each power supply hardware for control, monitoring, and communicating to the host computer. One PSCU can control as many as eight correction magnet power supplies.

It was planned to use a 13-bit DAC (with a shunt) for the reference signal generation, however it may be necessary to use a higher resolution DAC (maybe 16-bit). In that case a CT will be required for the magnet current measuring device. The host computer supplies a current value to the PSCU, and it sends out a pulse train to the DAC to set the dc-to-dc converter's output current. This current is the average (bias) correction current, and the current setting is done with open loop. The host computer can then modulate the correction magnet's current by counting the DAC UP and DOWN for the dynamic correction. This dynamic correction is done with closed feedback loop. The host computer will sense the correction magnet field, and manipulate it to compensate for the attenuation and phase delay due to the eddy current effect of the vacuum chamber [2].

Figure 4 shows the simplified regulator circuit to generate gating signals. The reference signal, V_r , from the DAC is 0 to +5V for the positive magnet current and 0 to -5V for negative

current. A polarity signal, which determines a set of switches to be controlled, is derived from the reference signal by using a comparator. If it is a positive value, then a high signal is obtained. Similarly if it is a negative value, a low signal is obtained. The feedback signal, V_f , is provided from a current measuring device. Assuming 16-bit DACs are required for storage ring correction magnets, a zero-flux CT provides +10V (-10V) for maximum positive (negative) current. This +/- 10V signal is reduced by half to match with the reference signal, V_r . The output of the error amplifier, V_e , is compared with a saw tooth signal, V_s , which is synchronized with the master clock, at a comparator, generating a pulse train. This PWM signal is combined with the polarity signal using an AND gate to determine which switch S1 or S2 is to be controlled. The maximum pulse width could be 100%, however, in general, it is 50% at minimum input voltage and full load current for dc correction current, leaving the remaining 50% for the dynamic correction.

4.2 Control for injector synchrotron correction magnets

Basically the same circuits as in the storage ring correction magnets apply to the injector synchrotron. The differences will be described in this subsection. For injector synchrotron correction magnets, a 12-bit DAC is used for the reference signal, and a shunt resistor is used for the current measuring device, developing about 0.2V across the shunt at full magnet current. Thus, this signal needs to be amplified and isolated prior to the error amplifier input terminal.

As explained in the Introduction, an AFG is used to generate the reference correction signal, V_r , for injector synchrotron correction magnets. The AFG is located in the PSCU, and its design is based on scanning out encoded data from a semi-conductor memory, a first-in-first-out (FIFO) device. The AFG input data consists of a maximum of 20 correction values randomly spaced within the injector synchrotron acceleration window (250 ms). Additional points between these values are then linearly interpolated to create a uniformly spaced 1000 data-point function stored in the FIFO. Each point is scanned out in synchronism with the acceleration cycle, and used to clock an up/down counter driving the DAC. Since the function data is first stored before use, its effect is a feedforward (open loop) correction. The optimum function for each correction magnet is determined via an iterative process based on the beam position during machine tune-up. Figure 5 shows the correction magnet timing in an injector synchrotron cycle (500 ms). The FIFO empty flag signal is generated when the read pointer equals the write pointer. After beam extraction the FIFO read pointer is returned to location 0 to prepare for the next scan cycle. The interval between the empty flag signal and the following injection signal is reserved for

returning the DAC output to its DC bias level, and for the update of FIFO data if an update request signal is present.

4.3 Control for PAR correction magnets

Since PAR correction magnets do not require any dynamic correction, only dc bias level information is received from the host computer. Therefore the same power supply as for injector synchrotron, (i.e. Type III BPS), is used , except that the PSCU does not include an AFG.

5. DRIVE

Although the drive requirements for power MOSFETs are relatively simple compared with the equivalent bipolar transistors, some considerations are needed for high-current power MOSFETs. The input capacitances of high-current power MOSFETs are quite large, for example it is approximately 20 nF for a 200-A MOSFET. This is perhaps an order of magnitude higher than the typical TO-3 or TO-220 power MOSFET, and it has a definite impact on the driver design. When high currents are switched at high speed, the parasitic circuit inductances inevitably associated with a practical circuit. At drain currents greater than 50 A, a di/dt on the order of 5 A/ns is readily achievable. At this speed, parasitic circuit inductances become first-order determinants of performance for 200-A MOSFETs. In the circuit shown in Figure 6, as drain current is increased, di/dt increases also. Consequently, the higher di/dt causes a larger voltage development across the parasitic inductance, L_s . At turn-off, this voltage positively biases the gate, and hence increases crossover time. If the voltage developed across, L_s , is countered by negative gate bias, crossover time is decreased [3]. Therefore, for storage ring correction magnet power supplies, Type I and II BPSs, a negative gate bias of -5 V is applied to the switch S1 (S2) during OFF time. But for Type III BPSs only the positive gate signal from an IC MOSFET driver is applied to the switch.

6 PROTECTIONS

6.1 Input capacitor protection

When both switches S1 and S4 (or S2 and S3) are turned OFF due to any undesired failure, the energy stored in the magnet has to be dumped into the input capacitor via the anti-parallel

diodes D2 and D3 (or D1 and D4). In this case, the equivalent circuit is shown in Fig. 7, and the equation for this figure is written as

$$\frac{1}{C_i} \int i(t) dt + L_m \frac{di(t)}{dt} + R_m i(t) + 2V_D = 0 \quad (8)$$

where C_i = input capacitance.

By solving (8) for $i(t)$, we obtain

$$i(t) = \frac{e^{-\alpha t}}{\beta} \left\{ \beta I_{Lf} \cos \beta t - \left(\alpha I_{Lf} + \frac{V_k}{L_m} \right) \sin \beta t \right\} \quad (9)$$

where

$$\alpha = \frac{-R_m}{2L_m}, \quad \beta = \sqrt{\frac{1}{L_m C_i} - \frac{R_m^2}{4L_m^2}},$$

I_{Lf} = initial magnet current at the time both switches S1 and S4

(or S2 and S3) are turned OFF,

$V_k = V_{cf} - 2V_D$, and

V_{cf} = initial voltage across the input capacitor C_i at the time both switches S1 and S4 (or S2 and S3) are turned OFF.

Thus, the voltage across the input capacitor, V_c , is given by

$$\begin{aligned} V_c &= \frac{1}{C_i} \int i(t) dt \\ &= \frac{e^{-\alpha t}}{\beta} \left\{ \beta V_k \cos \beta t + \left(\alpha V_k + \frac{I_{Lf}}{C_i} \right) \sin \beta t \right\} \end{aligned} \quad (10)$$

(9) and (10) are plotted in Fig. 8 for the case of Vertical Correction Sextupole as an example.

The values used are:

$$\begin{aligned} L_m &= 0.086 \text{ H}, \quad R_m = 0.187 \text{ } \Omega, \quad C_i = 4 \times 5,600 \text{ } \mu\text{F}/100\text{V}, \\ V_D &= 1.5 \text{ V}, \quad V_{co} = V_{in} = 50 \text{ Vdc}, \quad \text{and} \quad I_{Lf} = I_o = 113 \text{ Adc}. \end{aligned}$$

As we can see from the figure, the input capacitor voltage reaches about 240 V, which exceeds the input capacitor's voltage rating. Therefore, the input capacitor must be protected from exceeding its voltage rating.

The idea here to limit the input capacitor voltage is as follows. Whenever the power supplies need to be shut down due to any fault condition, we need to make sure that the upper switch S1 (or S2) is opened first, and the bottom switch S4 (or S3) is opened some time later to allow the magnet current to decay through the normal freewheeling path and not through the input capacitor. Also, the input bus voltage is monitored to limit it in the case that both switches S1 and S4 (or S2 and S3) are opened unintentionally, due to bias supply failure, for example. If the input voltage exceeds a predetermined threshold level, a high signal for a certain period is generated and OR-ed with the polarity signal, in order to ensure the bottom switch S4 (or S3) conducts for some period, allowing the magnet current to decay through the normal freewheeling path.

6.2 Monitoring and Interlocks

In order to protect the power supply system, the monitoring circuitry monitors some important parameters, such as magnet current, input bus voltage, temperatures of switches, cooling water temperature and pressure, and bias supply condition. If any fault condition is detected, a shut down signal is generated to disable the gating signals.

7. REFERENCES

- [1] O. D. Despe, "Arbitrary Function Generator for APS Injector Synchrotron Correction Magnets," ANL Light-Source Note, LSN-158, November 1990.
- [2] W. Praeg, "Frequency Response of Storage Ring Magnets, Eddy Current Shielding of Vacuum Chamber," ANL Light-Source Note, LSN-45, December 1985.
- [3] W. Schultz, "Multichip Power MOSFETs Beat Bipolars at High - Current Switching," Electronic Design, pp. 223- 232, June 1984.

Table 1: Summary of correction magnet power supplies for the APS machine.

					Rating			$\Delta I/I_{\max}$				Ref. Res. [bit]
Correction Magnets		No. of Units	L [H]	R [Ω]	I [A]	V [V]	P [kW]	Tracking Error	Ripple Current	Stability	Reprodu- cibility	
Storage Ring	Vert. Corr. Sextupole	280	0.086	0.187	113	21.13	2.39	5×10^{-4}	1×10^{-3}	3×10^{-4}	6×10^{-4}	13
	Hori. Corr. Dipole	240	0.0122	0.12752	90	11.48	1.03	7×10^{-4}	"	"	"	"
	Skew Quadrupole	20	0.0122	0.12752	90	11.48	1.03	"	"	"	"	"
	Trim Dipole Coil	80	0.016	0.234	54	12.64	0.68	"	"	"	"	"
	H. & V. Corr. Dip. : H.	78	0.003	0.095	134	12.73	1.71	"	"	"	"	"
	" : V.	78	0.004	0.133	116	15.43	1.79	"	"	"	"	"
Injector	H. & V. Corr. Dip. : H.	40	0.47	1.378	21	28.94	0.61	4×10^{-3}	"	"	"	12
Synch.	" : V.	40	0.106	2.422	17	41.17	0.70	"	"	"	"	"
PAR	H. & V. Correction	20	0.229	2.87	19	3.61	0.07	4×10^{-4}	"	"	"	"
	Trim Dipole	8	0.04	0.19	13	37.31	0.49	"	"	"	"	"

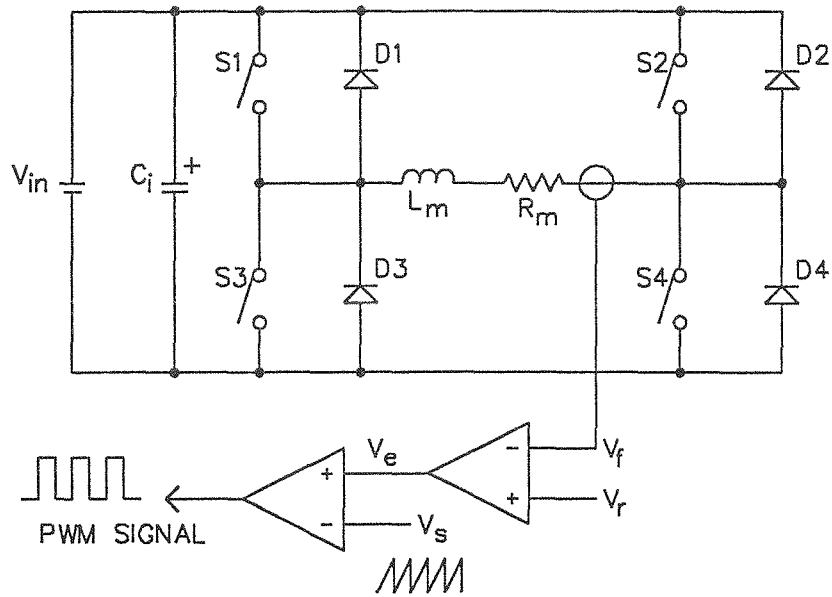


FIG. 1: SIMPLIFIED CIRCUIT OF A BIPOLAR POWER SUPPLY.

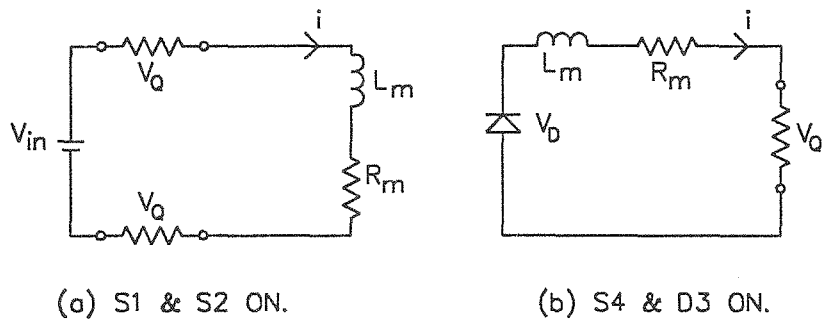


FIG. 2: EQUIVALENT CIRCUIT OF FIG. 1.

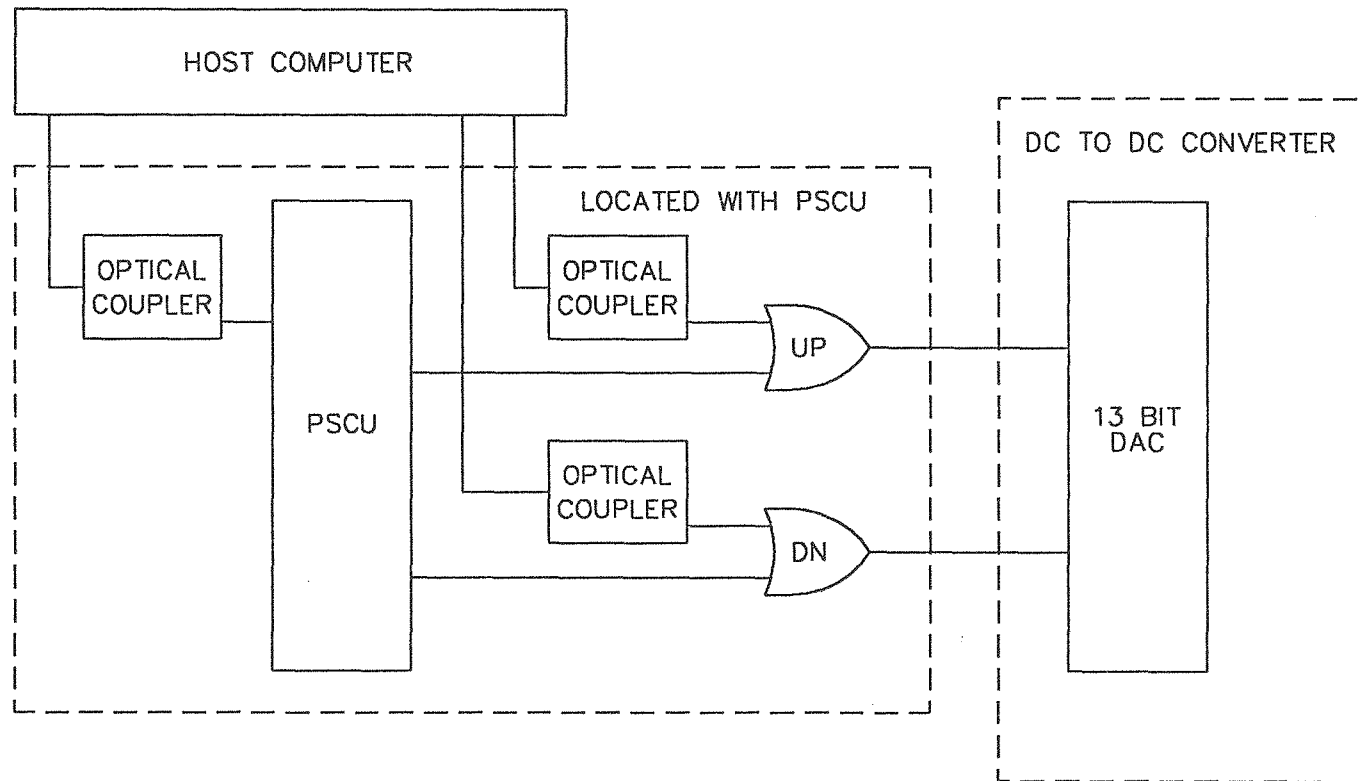


FIG. 3: SIMPLIFIED BLOCK DIAGRAM OF A CONTROL SCHEME.

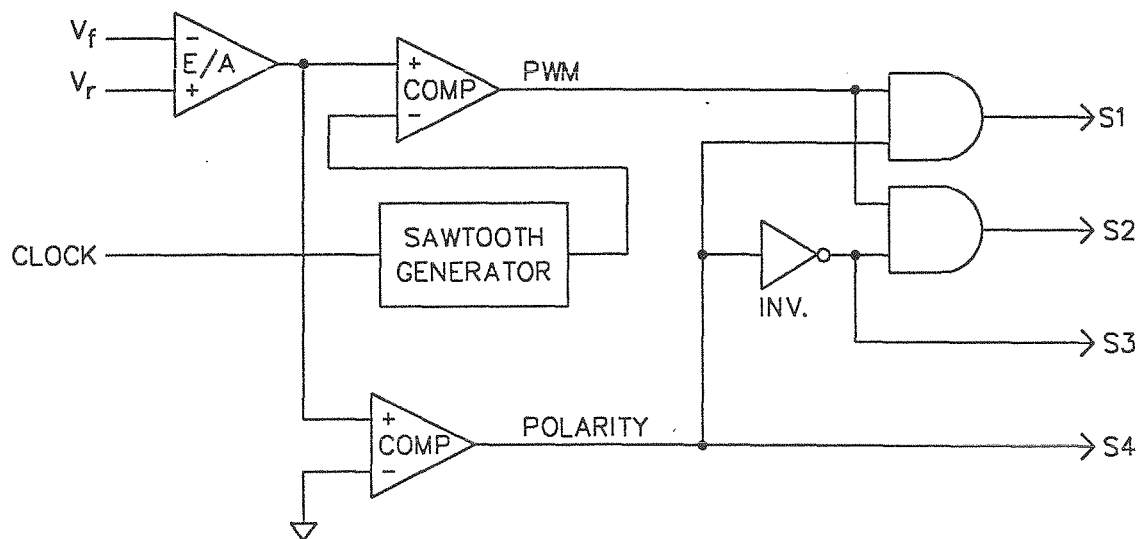


FIG. 4: SIMPLIFIED REGULATOR CIRCUIT.

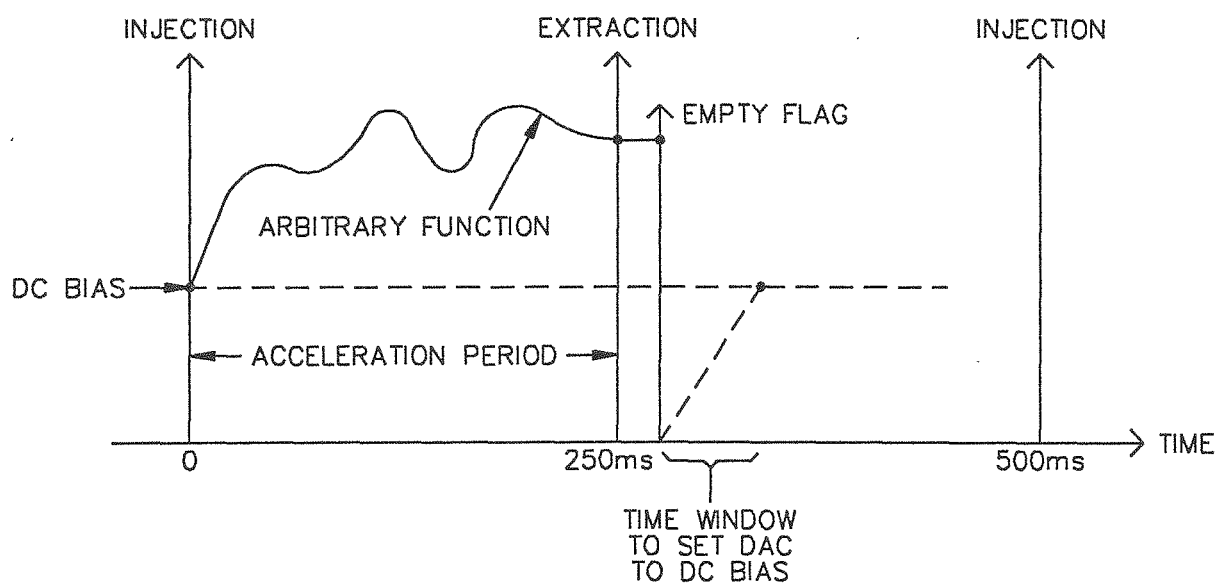


FIG. 5: ARBITRARY FUNCTION TIMING IN A SYNCHROTRON CYCLE.

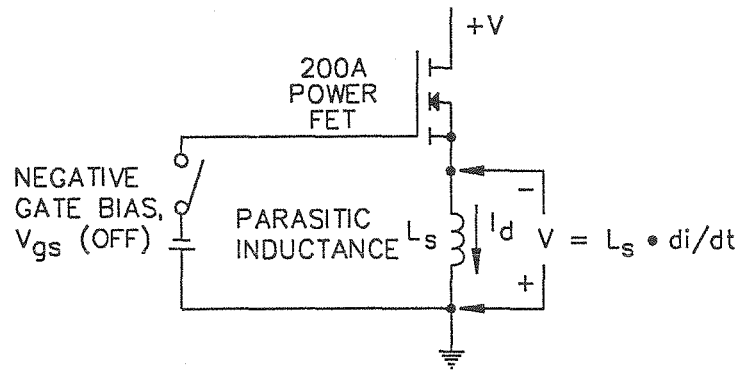


FIG. 6: THE di/dt EFFECTS IN PARASITIC INDUCTANCES FOR A 200A POWER MOSFET.

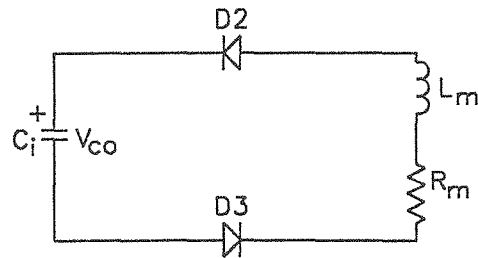


FIG. 7: EQUIVALENT CIRCUIT WHEN S1 & S4 OFF.

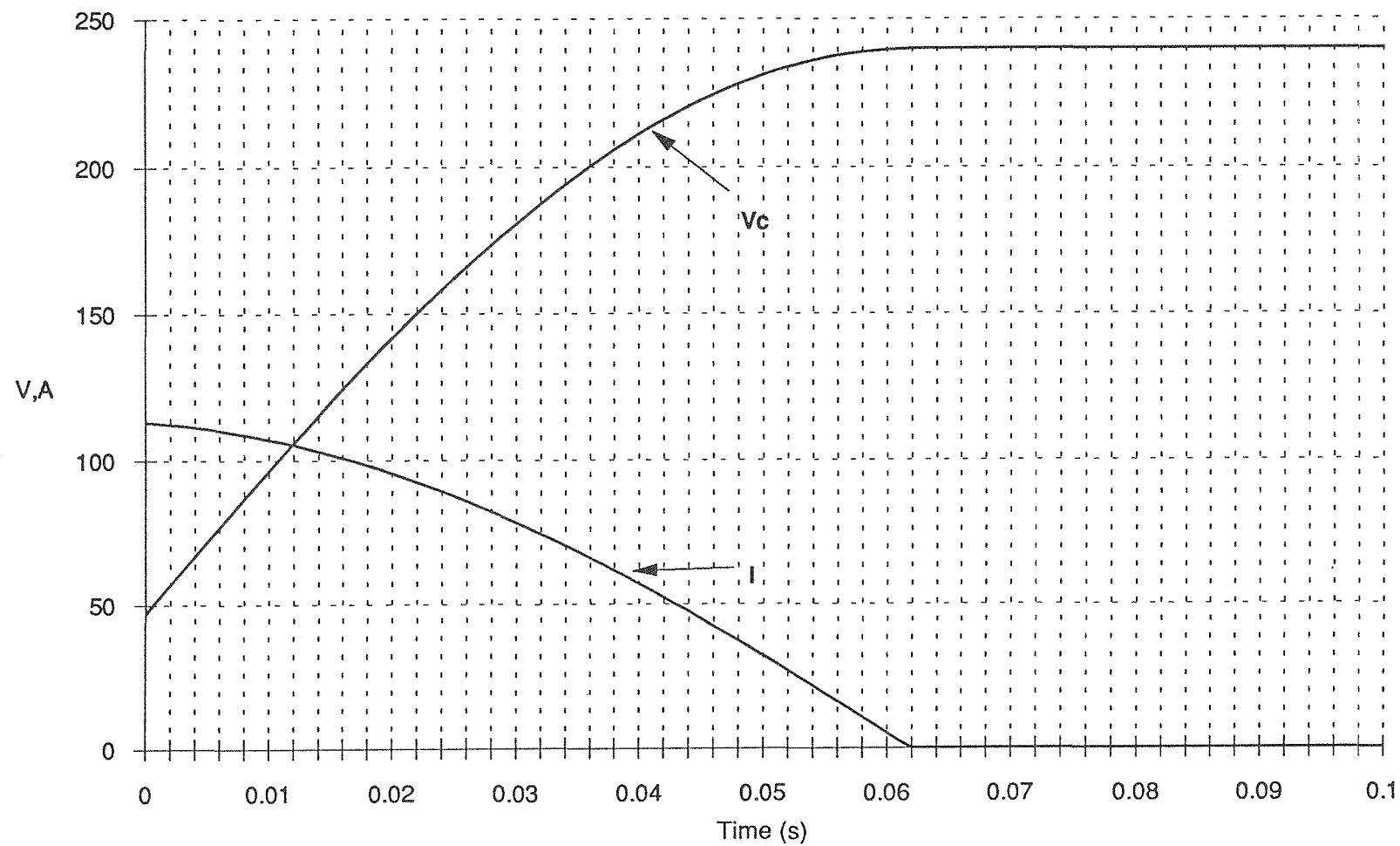


Fig.8: A plot of I and V_c when S_1 and S_4 OFF.